Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	(("5678567") or ("5771370")).PN.	USPAT	OR	OFF	2005/07/19 13:36
L2	35	optimize and hardware and software and co-simulation	USPAT	OR	OFF	2005/07/19 13:34
L3	37	optimize and hardware and software and co-simulation	USPAT	OR	ON	2005/07/19 13:34
L4	2	(("5768567") or ("5771370")).PN.	USPAT	OR	OFF	2005/07/19 13:37
L5	0	4 and (cycle adj accurate)	USPAT	OR	ON	2005/07/19 13:37
L6	0	4 and (cycle-accurate)	USPAT	OR	ON	2005/07/19 13:37
L7	0	4 and (cycle-accurate)	USPAT	OR	ON	2005/07/19 13:39
L8	0	"09586433"	US-PGPUB	OR	OFF	2005/07/19 13:39
L9	0	"09/586,433"	US-PGPUB	OR	OFF	2005/07/19 13:39
L10	1	bortfeld.in.	US-PGPUB	OR	OFF	2005/07/19 13:43
L11	1	("6718294").PN.	USPAT	OR	OFF	2005/07/19 13:45
L12	1	(memory adj3 model) and (processor adj3 model) and software and (single adj3 (process or thread)) and (cycle adj3 accurate) and (function adj3 call)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/19 14:15
L13	1	"772140"	EPO	OR	ON	2005/07/19 14:17
L14	1	"867820"	EPO	OR	ON	2005/07/19 14:18
L15	1338	(703/15,13,21,22).CCLS.	USPAT	OR	OFF	2005/07/19 14:23
L16	32	15 and (cosimulation or co-simulation)	USPAT	OR	ON	2005/07/19 14:20
L17	4	16 and (cycle adj accurate)	USPAT	OR	ON	2005/07/19 14:20
L18	1810	(703/13,14,15,19,21,22).CCLS.	USPAT	OR	OFF	2005/07/19 14:23
L19	24	18 and (cycle adj3 accurate)	USPAT	OR	OFF	2005/07/19 14:24
L20	7	19 and (cosimulation or (co adj simulation) or (co-simulation))	USPAT	OR	ON	2005/07/19 14:24

Results for "(((coverification<in>metadata) <or> (co-verification<in>metadata))<and>(..."

Your search matched **14** of **59** documents.

A maximum of **100** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

» View Session History

» New Search

Modify Search

(((coverification<in>metadata) <or> (co-verification<in>metadata))<and>((coverific

☐ Check to search only within this results set

Display Format: ◉ Citation ○ Citation & Abstract

<and>("cycle accurate")

» **Key**

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Select **Article Information**

☐ 1. **Cycle and phase accurate DSP modeling and integration for HW/SW co-verificati**
Guerra, L.; Fitzner, J.; Talukdar, D.; Schlager, C.; Tabbara, B.; Zivojnovic, V.;
Design Automation Conference, 1999. Proceedings. 36th
21-25 June 1999 Page(s):964 - 969
AbstractPlus | Full Text: PDF(628 KB) **IEEE CNF**

☐ 2. **ArchC: a systemC-based architecture description language**
Rigo, S.; Araujo, G.; Bartholomeu, M.; Azevedo, R.;
Computer Architecture and High Performance Computing, 2004. SBAC-PAD 2004. 16t
27-29 Oct. 2004 Page(s):66 - 73
AbstractPlus | Full Text: PDF(160 KB) **IEEE CNF**

☐ 3. **Using SSDE for USB2.0 conformance co-verification**
Omnes, T.J.-F.; Postuma, G.; VerHaegh, J.; Boonen, M.; Gatherer, N.;
Formal Methods and Models for Co-Design, 2003. MEMOCODE '03. Proceedings. Firs
International Conference on
24-26 June 2003 Page(s):113 - 122
AbstractPlus | Full Text: PDF(738 KB) **IEEE CNF**

☐ 4. **A simulation based approach for incorporating virtual components IP cores into systems design**
Baganne, A.; Bennour, I.; Elmarzougui, M.; Martin, E.;
Acoustics, Speech, and Signal Processing, 2003. Proceedings. (ICASSP '03). 2003 IEI
Conference on
Volume 2, 6-10 April 2003 Page(s):II - 525-8 vol.2
AbstractPlus | Full Text: PDF(385 KB) **IEEE CNF**

☐ 5. **A multi-level design flow for incorporating IP cores: case study of 1D wavelet IP i**
Baganne, A.; Bennour, I.; Elmarzougui, M.; Gaiech, R.; Martin, E.;
Design, Automation and Test in Europe Conference and Exhibition, 2003
2003 Page(s):250 - 255 suppl.
AbstractPlus | Full Text: PDF(457 KB) **IEEE CNF**

☐ 6. **A simulation based approach for incorporating virtual components IP cores into systems design**
Beganne, A.; Bennour, I.; Elmarzougui, M.; Martin, E.;
Multimedia and Expo, 2003. ICME '03. Proceedings. 2003 International Conference on

Volume 2, 6-9 July 2003 Page(s):II - 817-20 vol.2
AbstractPlus | Full Text: PDF(372 KB) **IEEE CNF**

☐ **7. Models of IP's for automotive virtual integration platforms**
Giusto, P.; Ferrari, A.; Lavagno, L.; Sangiovanni-Vincentelli, A.; Brunel, J.-Y.; Fourgeau Guasto, E.;
Computer Design: VLSI in Computers and Processors, 2002. Proceedings. 2002 IEEE Conference on
16-18 Sept. 2002 Page(s):379
AbstractPlus | Full Text: PDF(218 KB) **IEEE CNF**

☐ **8. Hardware/software co-verification, an IP vendors viewpoint**
Hopes, T.;
Computer Design: VLSI in Computers and Processors, 1998. ICCD '98. Proceedings., Conference on
5-7 Oct. 1998 Page(s):242 - 246
AbstractPlus | Full Text: PDF(80 KB) **IEEE CNF**

☐ **9. Towards automating hardware/software co-design**
El-Kharashi, M.W.; El-Malaki, M.H.; Hammad, S.; Salem, A.; Wahdan, A.;
System-on-Chip for Real-Time Applications, 2004.Proceedings. 4th IEEE International
19-21 July 2004 Page(s):189 - 192
AbstractPlus | Full Text: PDF(250 KB) **IEEE CNF**

☐ **10. Native ISS-SystemC integration for the co-simulation of multi-processor SoC**
Fummi, F.; Martini, S.; Perbellini, G.; Poncino, M.;
Design, Automation and Test in Europe Conference and Exhibition, 2004. Proceedings
Volume 1, 16-20 Feb. 2004 Page(s):564 - 569 Vol.1
AbstractPlus | Full Text: PDF(424 KB) **IEEE CNF**

☐ **11. Verification of transaction-level SystemC models using RTL testbenches**
Jindal, R.; Jain, K.;
Formal Methods and Models for Co-Design, 2003. MEMOCODE '03. Proceedings. Firs International Conference on
24-26 June 2003 Page(s):199 - 203
AbstractPlus | Full Text: PDF(213 KB) **IEEE CNF**

☐ **12. Applying hardware/software co-design to systems-on-a-chip**
Berger, A.S.;
WESCON/98
15-17 Sept. 1998 Page(s):22 - 28
AbstractPlus | Full Text: PDF(608 KB) **IEEE CNF**

☐ **13. Logic and functional verification in a commercial semiconductor environment**
Kumar, J.; Pixley, C.;
Application of Concurrency to System Design, 1998. Proceedings., 1998 International
23-26 March 1998 Page(s):8 - 15
AbstractPlus | Full Text: PDF(36 KB) **IEEE CNF**

☐ **14. A system-level co-verification environment for ATM hardware design**
Post, G.; Muller, A.; Grotker, T.;
Design, Automation and Test in Europe, 1998., Proceedings
23-26 Feb. 1998 Page(s):424 - 428
AbstractPlus | Full Text: PDF(52 KB) **IEEE CNF**

View Selected Items

Results for "(coverification<in>metadata) <or> (co-verification<in>metadata)" e-mail
Your search matched **59** of **1194402** documents.
A maximum of **100** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

» View Session History
» New Search

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Modify Search

(coverification<in>metadata) <or> (co-verification<in>metadata)

☐ Check to search only within this results set

Display Format: ◉ Citation ○ Citation & Abstract

Select **Article Information** **View: 1-**

☐ **1. Target processor and co-verification environment independent adapter-a technol cycle-time for retargeting TI processor simulators in HW/SW co-verification envi**
Shah, R.; SubbaRao, R.;
ASIC/SOC Conference, 1999. Proceedings. Twelfth Annual IEEE International
15-18 Sept. 1999 Page(s):37 - 41
AbstractPlus | Full Text: PDF(312 KB) **IEEE CNF**

☐ **2. Hardware-software timing coverification of concurrent embedded real-time syste**
Hsiung, P.-A.;
Computers and Digital Techniques, IEE Proceedings-
Volume 147, Issue 2, March 2000 Page(s):83 - 92
AbstractPlus | Full Text: PDF(588 KB) **IEE JNL**

☐ **3. Hardware-software coverification of concurrent embedded real-time systems**
Pao-Ann Hsiung;
Real-Time Systems, 1999. Proceedings of the 11th Euromicro Conference on
9-11 June 1999 Page(s):216 - 223
AbstractPlus | Full Text: PDF(188 KB) **IEEE CNF**

☐ **4. Timing coverification of concurrent embedded real-time systems**
Hsiung, P.-A.;
Hardware/Software Codesign, 1999. (CODES '99) Proceedings of the Seventh Internat
on
3-5 May 1999 Page(s):110 - 114
AbstractPlus | Full Text: PDF(388 KB) **IEEE CNF**

☐ **5. Co-verification as risk management: minimizing the risk of incorporating a new p next embedded system design**
Kenney, J.;
Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Sy
Volume 6, 30 May-2 June 1999 Page(s):474 - 477 vol.6
AbstractPlus | Full Text: PDF(244 KB) **IEEE CNF**

☐ **6. Concurrent hardware/software coverification with Java threads**
Azizi, M.;
Parallel Computing in Electrical Engineering, 2002. PARELEC '02. Proceedings. Intern
Conference on

22-25 Sept. 2002 Page(s):95 - 98

AbstractPlus | Full Text: PDF(324 KB) **IEEE CNF**

☐ **7. Formal coverification of embedded systems using model checking**
Cortes, L.A.; Eles, P.; Peng, Z.;
Euromicro Conference, 2000. Proceedings of the 26th
Volume 1, 5-7 Sept. 2000 Page(s):106 - 113 vol.1

AbstractPlus | Full Text: PDF(660 KB) **IEEE CNF**

☐ **8. Methodology for hardware/software co-verification in C/C++**
Semeria, L.; Ghosh, A.;
Design Automation Conference, 2000. Proceedings of the ASP-DAC 2000. Asia and S
25-28 Jan. 2000 Page(s):405 - 408

AbstractPlus | Full Text: PDF(472 KB) **IEEE CNF**

☐ **9. Cycle and phase accurate DSP modeling and integration for HW/SW co-verificati**
Guerra, L.; Fitzner, J.; Talukdar, D.; Schlager, C.; Tabbara, B.; Zivojnovic, V.;
Design Automation Conference, 1999. Proceedings. 36th
21-25 June 1999 Page(s):964 - 969

AbstractPlus | Full Text: PDF(628 KB) **IEEE CNF**

☐ **10. Hardware/software co-verification, an IP vendors viewpoint**
Hopes, T.;
Computer Design: VLSI in Computers and Processors, 1998. ICCD '98. Proceedings., Conference on
5-7 Oct. 1998 Page(s):242 - 246

AbstractPlus | Full Text: PDF(80 KB) **IEEE CNF**

☐ **11. HW/SW CoVerification performance estimation and benchmark for a 24 embedde design**
Albrecht, T.W.; Notbauer, J.; Rohringer, S.;
Design Automation Conference, 1998. Proceedings
15-19 Jun 1998 Page(s):808 - 811

AbstractPlus | Full Text: PDF(352 KB) **IEEE CNF**

☐ **12. Simulation based system level fault insertion using co-verification tools**
Eklow, B.; Hosseini, A.; Chi Khuong; Pullela, S.; Vo, T.; Chau, H.;
Test Conference, 2004. Proceedings. International
26-28 Oct. 2004 Page(s):704 - 710

AbstractPlus | Full Text: PDF(695 KB) **IEEE CNF**

☐ **13. Hardware/Software co-verification platform for EOS design**
Peng Wang; Jinsong Liu; Lieguang Zeng;
ASIC, 2003. Proceedings. 5th International Conference on
Volume 1, 21-24 Oct. 2003 Page(s):195 - 198 Vol.1

AbstractPlus | Full Text: PDF(370 KB) **IEEE CNF**

☐ **14. Virtual in-circuit emulation for timing accurate system prototyping**
Benini, L.; Bruni, D.; Drago, N.; Fummi, F.; Poncino, M.;
ASIC/SOC Conference, 2002. 15th Annual IEEE International
25-28 Sept. 2002 Page(s):49 - 53

AbstractPlus | Full Text: PDF(434 KB) **IEEE CNF**

☐ **15. A debug sub-system for embedded-system co-verification**
Liu Jianhua; Zhu Ming; Bian Jinian; Xue Hongxi;
ASIC, 2001. Proceedings. 4th International Conference on
23-25 Oct. 2001 Page(s):777 - 780

AbstractPlus | Full Text: PDF(450 KB) **IEEE CNF**

☐ **16. Fast hardware-software coverification by optimistic execution of real processor**
Sungjoo Yoo; Jong-Eun Lee; Jinyong Jung; Kyungseok Rha; Youngchul Cho; Kiyoung
Design, Automation and Test in Europe Conference and Exhibition 2000. Proceedings
27-30 March 2000 Page(s):663 - 668
AbstractPlus | Full Text: PDF(88 KB) **IEEE CNF**

☐ **17. CVF-coverification framework**
Garcez, E.H.A.; Rosenstiel, W.;
Integrated Circuit Design, 1998. Proceedings. XI Brazilian Symposium on
30 Sept.-3 Oct. 1998 Page(s):103 - 106
AbstractPlus | Full Text: PDF(32 KB) **IEEE CNF**

☐ **18. A system-level co-verification environment for ATM hardware design**
Post, G.; Muller, A.; Grotker, T.;
Design, Automation and Test in Europe, 1998., Proceedings
23-26 Feb. 1998 Page(s):424 - 428
AbstractPlus | Full Text: PDF(52 KB) **IEEE CNF**

☐ **19. Effective Co-Verification of IEEE 802.11a MAC/PHY Combining Emulation and Si Technology**
IL-Gu Lee; Seung-Beom Lee; Sin-Chong Park;
Simulation Symposium, 2005. Proceedings. 38th Annual
04-06 April 2005 Page(s):138 - 146
AbstractPlus | Full Text: PDF(360 KB) **IEEE CNF**

☐ **20. ArchC: a systemC-based architecture description language**
Rigo, S.; Araujo, G.; Bartholomeu, M.; Azevedo, R.;
Computer Architecture and High Performance Computing, 2004. SBAC-PAD 2004. 16t
27-29 Oct. 2004 Page(s):66 - 73
AbstractPlus | Full Text: PDF(160 KB) **IEEE CNF**

☐ **21. Java based co-verification of expedited mobile device collaboration using obser**
Aly, S.G.; Salem, A.M.;
System-on-Chip for Real-Time Applications, 2003. Proceedings. The 3rd IEEE Internat
on
30 June-2 July 2003 Page(s):181 - 184
AbstractPlus | Full Text: PDF(222 KB) **IEEE CNF**

☐ **22. Using SSDE for USB2.0 conformance co-verification**
Omnes, T.J.-F.; Postuma, G.; VerHaegh, J.; Boonen, M.; Gatherer, N.;
Formal Methods and Models for Co-Design, 2003. MEMOCODE '03. Proceedings. Firs
International Conference on
24-26 June 2003 Page(s):113 - 122
AbstractPlus | Full Text: PDF(738 KB) **IEEE CNF**

☐ **23. Hardware software codesign of a safety-critical embedded computer system for endoscope**
Khan, G.N.; Jin, M.;
Electrical and Computer Engineering, 2002. IEEE CCECE 2002. Canadian Conference
Volume 2, 12-15 May 2002 Page(s):657 - 662
AbstractPlus | Full Text: PDF(867 KB) **IEEE CNF**

☐ **24. CAD flows for chip-package coverification**
Varma, A.K.; Glaser, A.; Franzon, P.D.;
Advanced Packaging, IEEE Transactions on [see also Components, Packaging and M

Technology, Part B: Advanced Packaging, IEEE Transactions on]
Volume 28, Issue 1, Feb 2005 Page(s):96 - 101

AbstractPlus | Full Text: PDF(480 KB) **IEEE JNL**

☐ **25. A demonstration of co-design and co-verification in a synchronous language**
Singh, S.;
Design, Automation and Test in Europe Conference and Exhibition, 2004. Proceedings
Volume 2, 16-20 Feb. 2004 Page(s):1394 - 1395 Vol.2

AbstractPlus | Full Text: PDF(189 KB) **IEEE CNF**

View Selected Items

View: 1-

Published before June 2000
Terms used
memory model processor software HDL unified simulation cycle accurate

Found **9** of **107,205**

Sort results by: relevance
Display results: expanded form

Save results to a Binder
Search Tips
Open results in a new window

Try an Advanced Search
Try this search in The ACM Guide

Results 1 - 9 of 9

Relevance scale

1 Formal verification in hardware design: a survey
Christoph Kern, Mark R. Greenstreet
April 1999 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 4 Issue 2
Full text available: pdf(411.53 KB) Additional Information: full citation, abstract, references, citings, index terms

In recent years, formal methods have emerged as an alternative approach to ensuring the quality and correctness of hardware designs, overcoming some of the limitations of traditional validation techniques such as simulation and testing. There are two main aspects to the application of formal methods in a design process: the formal framework used to specify desired properties of a design and the verification techniques and tools used to reason about the relationship between a spec ...

Keywords: case studies, formal methods, formal verification, hardware verification, language containment, model checking, survey, theorem proving

2 Technical reports
SIGACT News Staff
January 1980 **ACM SIGACT News**, Volume 12 Issue 1
Full text available: pdf(5.28 MB) Additional Information: full citation

3 High-level design verification of microprocessors via error modeling
D. Van Campenhout, H. Al-Asaad, J. P. Hayes, T. Mudge, R. B. Brown
October 1998 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 3 Issue 4
Full text available: pdf(174.30 KB) Additional Information: full citation, abstract, references, citings, index terms

A design verification methodology for microprocessor hardware based on modeling design errors and generating simulation vectors for the modeled errors via physical fault testing techniques is presented. We have systematically collected design error data from a number of microprocessor design projects. The error data is used to derive error models suitable for design verification testing. A class of basic error models is identified and shown to yield tests that provide good coverage of comm ...

Keywords: design errors, design verification, error modeling

4 A Multi-Level Transformation Approach to HW/SW Codesign: A Case Study
Tommy King-Yin Cheung, Graham Hellestrand, Prasert Kanthamanon
March 1996 **Proceedings of the 4th International Workshop on Hardware/Software Co-Design**
Full text available: pdf(970.93 KB) Publisher Site
Additional Information: full citation, abstract, citings

This reported work applies a transformational synthesis approach to hardware/software codesign. In this approach, the process of algorithm design is coupled early on with hardware design to allow for a complete design space exploration. Both the specification and the transformation mechanisms are encoded in a functional notation, called form, which facilitates algorithmic derivation, structural transformation and verification. In the algorithmic derivation phase, possible computational schedules ...

Keywords: Functional Languages, Design Transformations.

5 An architecture design and assessment system for software/hardware codesign
Connie U. Smith, Geoffrey A. Frank, John L. Cuadrado
June 1985 **Proceedings of the 22nd ACM/IEEE conference on Design automation**
Full text available: pdf(908.59 KB) Additional Information: full citation, abstract, references, citings, index terms

Codesign of hardware and software for high performance signal processing systems is important if the potential benefits of VLSI are to be realized. This article describes a CAD system developed to support the codesign of hardware and software architectures for high performance digital signal processors which is based on a directed graph methodology. A comprehensive example is developed to demonstrate the use of the system, the fundamentals of the modeling and analysis methodology are discus ...

6 High-level scheduling model and control synthesis for a broad range of design applications
Chih-Tung Chen, Kayhan Küçükçakar
November 1997 **Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(110.32 KB) Publisher Site
Additional Information: full citation, abstract, references, citings, index terms

This paper presents a versatile scheduling model and an efficient control synthesis methodology which enables architectural (high-level) design/synthesis systems to seamlessly support a broad range of architectural design applications from datapath-dominated digital signal processing (DSP) to micro-processors/controllers and control-dominated peripherals, utilizing multi-phase clocking schemes, multiple threading, data-dependent delays, pipelining, and combinations of the above. The work present ...

Keywords: control synthesis, scheduling model, multi-phase clocking, multi-threading, pipelining, relative scheduling, high-level synthesis, architectural synthesis, behavioral synthesis, architectural power optimization.

7 High-level synthesis and codesign methods: an application to a videophone codec
Pierre Paulin, Jean Fréhel, Michel Harrand, Elisabeth Berrebi, Clifford Liem, François Naçabal, Jean-Claude Herluison
December 1995 **Proceedings of the conference on European design automation**

Full text available: pdf(798.30 KB) Additional Information: full citation, references, citings, index terms

8 Enhancing simulation with BDDs and ATPG
Malay K. Ganai, Adnan Aziz, Andreas Kuehlmann
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**
Full text available: pdf(795.60 KB) Additional Information: full citation, references, citings, index terms

Keywords: ATPG, BDDs, coverage, formal verification, simulation

9 Standards for system-level design: practical reality or solution in search of a question?
Christopher K. Lennard, Patrick Schaumont, Gjalt de Jong, Anssi Haverinen, Pete Hardee
January 2000 **Proceedings of the conference on Design, automation and test in Europe**
Full text available: pdf(74.65 KB) Additional Information: full citation, references, citings, index terms
Publisher Site

Results 1 - 9 of 9